Launched by Motorola
freescale semiconductor

FACSIMILE

RECEIVED
CENTRAL FAX CENTER
JUN 28 2005

LAW DEPARTMENT
FREESCALE SEMICONDUCTOR, INC.

DATE: June 28, 2005

TO: MS: Appeal Briefs - Patents (ADDRESSEE) (EXTENSION)

USPTO (703) 872-9306
(LOCATION) (FAX NUMBER)

FROM: Stacie Herrera for Robert L. King (512) 996-6848
(SENDER) (EXTENSION)

TOTAL NUMBER OF PAGES 21 **(including this page)**

IF YOU HAVE ANY TROUBLE OR QUESTIONS WITH TRANSMISSION, OR HAVE RECEIVED IT IN ERROR, PLEASE CALL:(512) 996-6839

ALL ITEMS MARKED WITH AN "X" ARE INCLUDED:

1.	x	1 page Facsimile Cover Sheet
2.	x	2 page Response to Notice of Non-Compliant Appeal Brief
3.	x	18 page Appeal Brief

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING FACSIMILE TRANSMITTED TO THE PATENT AND TRADEMARK OFFICE:

ON: 6/28/05 (Date) Stacie Herrera (Signature)

FREESCALE LAW DEPARTMENT
7700 W. PARMER LANE MD: TX32/PL02
AUSTIN, TEXAS 78729
Fax Number (512) 996-6854

NOTICE: This facsimile transmission may contain information that is confidential, privileged or exempt from disclosure under applicable law. It is intended only for the person to whom it is addressed. Unauthorized use, disclosure, copying or distribution may expose you to legal liability. If you have received this transmission in error, please immediately notify us by telephone (collect) to arrange for return of the documents received and any copies made. Thank you.

PLEASE GIVE THESE PAPERS TO:

EXAMINER: Christain Chase
GROUP ART UNIT: 2189
SERIAL NO.: 10/600,959
FILED: JUNE 20, 2003
INVENTOR: AFZAL MALIK ET AL

RECEIVED
CENTRAL FAX CENTER
JUN 28 2005

DOCKET NO. SC12865TH

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT	Afzal Malik et al.	GROUP ART UNIT:	2189
APPLN. NO.:	10/600,959	EXAMINER:	Christian Chace
FILED:	June 20, 2003	CONFIRMATION No.:	6580
TITLE:	METHOD AND APPARATUS FOR DYNAMIC PREFETCH BUFFER CONFIGURATION AND REPLACEMENT		

Certificate of Transmission under 37 C.F.R 1.8

I hereby certify that this correspondence is being facsimile transmitted to the Patent and Trademark Office.
on June 28, 2005

Stacie Herrera

Signature

Stacie Herrera

Printed Name of Person Signing Certificate

RESPONSE TO NOTICE OF NON-COMPLIANT APPEAL BRIEF

COMMISSIONER FOR PATENTS
ALEXANDRIA, VA 22313
BOARD OF PATENT APPEALS & INTERFERENCES:

Applicants were notified in a communication mailed June 10, 2005 of a failure to comply with one or more provisions of 37 CFR 41.37 in connection with the Appeal Brief filed on April 13, 2005. Applicants are herein correcting the specified items of non-compliance and submitting a complete new brief that is compliant with 37 CFR 41.37. The only changes made to the attached compliant Appeal Brief from the original filed Appeal Brief relate to changes required to become compliant with 37 CFR 41.37.

In particular, the corrected Appeal Brief submitted herewith refers to the specification by page and line number in the "Summary of claimed subject matter". Further, the first question for consideration is rephrased to recite whether the rejected claims are anticipated by the art made of

record as opposed to being made obvious. Additionally, the third question concerning grounds for rejection is removed since the issue was not a basis for rejection of the claims.

Applicants therefore request the acceptance of the attached timely filed Appeal Brief and the withdrawal of the objection for not being compliant with 37 CFR 41.37.

Respectfully submitted,
AFZAL MALIK et al.

Robert L. King

Robert L. King
Attorney for Appellants
Reg. No. 30,185
Ph: (512) 996-6839

PAGE 3/21 * RCVD AT 6/28/2005 5:52:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:5129966854 * DURATION (mm-ss):05-58

RECEIVED
CENTRAL FAX CENTER
JUN 28 2005

DOCKET NO. SC12865TH

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT	Afzal Malik et al.	GROUP ART UNIT:	2189
APPLN. NO.:	10/600,959	EXAMINER:	Christian Chace
FILED:	June 20, 2003	CONFIRMATION No.:	6580
TITLE:	METHOD AND APPARATUS FOR DYNAMIC PREFETCH BUFFER CONFIGURATION AND REPLACEMENT		

Certificate of Transmission under 37 C.F.R 1.8

I hereby certify that this correspondence is being facsimile transmitted to the Patent and Trademark Office.
on June 28 2005

Stacie Herrera
Signature

Stacie Herrera
Printed Name of Person Signing Certificate

APPEAL BRIEF

COMMISSIONER FOR PATENTS
ALEXANDRIA, VA 22313
BOARD OF PATENT APPEALS & INTERFERENCES:

This brief is filed in the matter of the Appeal to the Board of Appeals and Interferences of the rejection of the claims of the above-referenced application for patent.

REAL PARTY IN INTEREST

The present application is wholly assigned to FREESCALE SEMICONDUCTOR, INC., with its headquarters in Austin, Texas.

RELATED APPEALS AND INTERFERENCES

Appellants are unaware of other appeals or interferences which will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Claims 1-10 and 13-22 are pending in the application and claims 1-10 and 13-19 are involved in this appeal as claims 20-22 are allowed. Claim 1 was previously presented. Claim 2 is original. Claim 3 was previously presented. Claims 4-7 are original. Claim 8 was previously presented. Claims 9 and 10 are original. Claims 11 and 12 have been canceled. Claim 13 is original. Claim 14 was previously presented. Claim 15 is original. Claim 16 was previously presented. Claims 17-19 are original. Claim 20 was previously presented. Claims 21 and 22 are original. Claims 23 and 24 have been canceled.

Claims 1-6, 8-10, 13-16 and 19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Peters et al., U.S. Patent No. 6,636,927 (Peters et al.). Claims 17 and 18 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Peters et al. (cited supra) in view of Hicks et al., U.S. Patent No. 6,085,291.

The rejection of claims 1-6, 8-10 and 13-19 is being appealed.

STATUS OF AMENDMENTS

A most recent amendment filed on January 19, 2005 was entered. A final rejection was mailed on April 4, 2005. No further amendments were filed after the final rejection.

PAGE 5/21 * RCVD AT 6/28/2005 5:52:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:5129966854 * DURATION (mm-ss):05-58

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 recites a method for configuring a prefetch buffer (30 of FIGs. 1-3). A read request to read the buffer is received from a master (step 82 of FIG. 6) as described on page 10, lines 12-13. In response to the read request the total length of at least one of the prefetch buffer lines is selectively modified based on an attribute of the read request (emphasis added). A discussion of a read request is at page 5, lines 14-20. Modification of buffer line size is discussed at page 6, lines 3-6, page 13, lines 19-21, the Abstract, page 22, lines 10-12 and elsewhere. An adjusted line size is created. The selective modification of total length of a buffer line eliminates dedication of buffer storage that is unused. As a result, the prefetch buffer has lines that have differing total length during operation as can be readily seen in FIG. 3 and described at page 8, lines 4-7 of Appellants' specification.

Independent claim 14 also recites a method for configuring a prefetch buffer (30 of FIGs. 1-3). A read request to a memory is provided from a requesting master (step 82 of FIG. 6) as described on page 10, lines 12-13. The read request has a corresponding data size and burst length as described at page 5, lines 19 and 20. A buffer reconfiguration indicator (page 10, line 26 to page 11, line 5 and 74 of FIG. 5) is provided based on the data size and the burst length. A replacement entry within the buffer is selected as described at page 9, lines 15-17. Based on the buffer reconfiguration indicator the total length of the replacement entry is selectively modified as discussed at page 6, lines 3-6, page 13, lines 19-21, the Abstract, page 22, lines 10-12 and elsewhere. The selective modification of the replacement entry is based on an attribute of the read request. In claim 14, the attribute is data size and burst length. The adjusted line size is recited to eliminate dedicating unused buffer storage to the replacement entry of the prefetch buffer, page 13, line17 to page 14, line 2 and FIGs. 2 and 3. Data fetched from the memory is

PAGE 6/21 * RCVD AT 6/28/2005 5:52:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:5129966854 * DURATION (mm-ss):05-58

then stored in the replacement entry of the buffer as described in step 136 of FIG. 8 and page 13, lines 11-12.

PAGE 7/21 * RCVD AT 6/28/2005 5:52:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:5129966854 * DURATION (mm-ss):05-58

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1) Are claims 1-6, 8-10, 13-16 and 19 anticipated by Peters et al. (U.S. Patent 6,636,927)?

2) Are claims 17 and 18 made obvious in view of the combination of Peters et al. (U.S. Patent 6,636,927) and Hicks et al. (U.S. Patent 6,085,291)?

ARGUMENT

Arguments for Ground 1

Independent Claim 1

Independent claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Peters et al. The rejection is based on characterizing the Peters et al. patent as teaching "selectively modifying a 'total length of one (or more) prefetch buffer lines" (data size) of the prefetch buffer based on an attribute of the read request to an adjusted line size". Appellants respectfully submit that Peters et al. disclose a plurality of prefetch buffers having master-specific prefetch sizes so that a prefetch buffer of fixed and non-varying size exists for each master. See for example Col. 3, lines 40-41 and Col. 10, lines 10-13. See also Col. 9, lines 60-63, which states in connection with FIG. 7 that "Each of the read and write prefetch buffers 702 and 704 includes a plurality of segments, each of which is adapted to store data for one master device." (emphasis added). The drawing in FIG. 7 of the Peters et al. patent shows the buffers 702 and 704 to have a fixed, non-varying line size.

In the Peters et al. system, predetermined fixed buffer line sizes are correlated respectively to bus masters operating with known data sizes. Control circuitry identified as bridge control circuitry and a prefetch control register is required in the system disclosed by

PAGE 8/21 * RCVD AT 6/28/2005 5:52:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:5129966854 * DURATION (mm-ss):05-58

Peters et al. to correlate a predetermined prefetch buffer segment with a predetermined bus master based upon size information that is correlated in a configuration or routing register. Each buffer segment of the Peters et al. system has a fixed data size optimized for one master device. See Col. 9, lines 60-67. An arbiter is required to determine which prefetch control register is associated with a master device and the control circuitry selects and accesses the associated prefetch control register. See Col. 8, lines 31-36.

Variations disclosed by Peters et al. include the ability to program the control registers to change size and assigned master. See Col. 7, lines 29-31. However, once the control registers are programmed, the prefetch register size is fixed for a specific assigned master for all reads and writes. Another variation disclosed by Peters et al. is to store various prefetch size information corresponding to the size or amount of data that is prefetched from a source for various data commands. See Col. 7, lines 20-43. This use of the Peters et al. configuration register is for controlling how much data is stored in or retrieved from a static size buffer as opposed to selectively modifying length of the buffer lines in response to the command. In all examples, Peters et al. disclose a configuration register that is used to correlate a fixed prefetch buffer size to a defined device or transfer command.

In contrast, claim 1 recites a method for configuring a prefetch buffer by "selectively modifying total length of one or more prefetch buffer lines of the prefetch buffer" that is "in response to the read request" and "based on an attribute of the read request". The method of claim 1 avoids the necessity of having various fixed-size prefetch buffers, each of differing size, to efficiently interface with multiple bus masters. As recited in claim 1, the total length of a prefetch buffer line is selectively modified in response to a read request from a master. This claim recital is distinguished from the Peters et al. system that routes data to a specific prefetch buffer segment in response to a read request.

Each buffer line of the prefetch buffer in claim 1 has dynamic length that varies with program flow. Comparing FIG. 7 of the Peters et al. patent with FIG. 3 of the present application

PAGE 9/21 * RCVD AT 6/28/2005 5:52:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:5129966854 * DURATION (mm-ss):05-58

clearly illustrates the claimed difference. Claim 1 recites that a total length of a buffer line is selectively modified in response to a read request. As a result, with the recited method of claim 1 multiple bus masters may efficiently use a same portion of a prefetch buffer. In contrast, in the Peters et al. system significantly more buffer storage must be dedicated to adequately serve multiple bus masters in an efficient manner. Because the Peters et al. system functions to route data to a predetermined fixed size line of a prefetch buffer determined by which requesting device originates the operation, the recitals of claim 1 are neither taught nor suggested by Peters et al. Appellants therefore request the reversal of the rejection of claim 1 under 35 U.S.C. 102(e).

Dependent claims 2-6, 8-10 and 13

Dependent claims 2-6, 8-10 and 13 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Peters et al. Each of these claims is patentable over Peters et al. at least as a result of being dependent from claim 1 for the reasons provided above. In claim 2 the attribute of the read request is recited as being one of three attributes including "a master identifier corresponding to the master". In the Peters et al. system, clearly there is information which identifies which master requests an action. In the Peters et al. system the circuitry referred to as the bridge control circuitry must then correlate the master identity in the size configuration register. The result of that correlation is to route the master's request to a specific fixed size prefetch buffer for that master. In contrast, claim 2 recites using the master's identity to selectively modify a prefetch buffer line length when the master generates a read request. The Peters et al. patent does not teach or suggest this function. Claim 2 also recites using a data size of the read request and a burst length of a read request to selectively modify a prefetch buffer line length. These features are not taught by Peters et al.

Dependent claim 3 recites using two attributes of a read request to selectively modify a prefetch buffer line length. While the Peters et al. system uses master identity and size

PAGE 10/21 * RCVD AT 6/28/2005 5:52:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:5129966854 * DURATION (mm-ss):05-58

information to determine which previously sized buffer to use, these features of the Peters et al. system do not teach or suggest the combination of claims 1, 2 and 3 as recited in claim 3.

Dependent claim 4 recites that the read request is a miss in the prefetch buffer. Appellants note that data misses in memory and storage devices are well known in this art. The rejection of claim 3 is based on Col. 4, lines 38-40 of Peters et al. which state that data is provided from the prefetch buffer associated with a requesting first device when data is present. In contrast, dependent claim 4 recites that a prefetch buffer line size is selectively modified when there is a miss in the buffer consistent with the embodiment illustrated in FIG. 6, step 84 et seq. Peters et al. do not teach the recitals of claims 4 and 1 at Col. 4, lines 38-40.

Dependent claim 5 recites that the prefetch buffer has a plurality of lines that each have a status field. The rejection of claim 5 is based on the disclosed configuration registers of Peters et al. The only mention of the word "status" in the Peters et al. patent is at Col. 8, line 1 in connection with PCI status information required for communication that is stored in the configuration registers of the bridge control circuitry taught therein. In Figure 3 of the Peters et al. patent, it is clear that configuration registers 308 are separate and distinct from the prefetch buffer 304. Further, a configuration register is illustrated in detail separate from the prefetch buffer in Figures 6 and 7. Therefore, Peters et al. clearly do not disclose a prefetch buffer having lines with a status field.

Dependent claim 6 recites that at least a portion of the buffer lines are selected as replacement entries based on the status fields of the buffer. Because the prefetch buffer in the Peters et al. patent does not have lines with a status field included therein, claim 6 is readily distinguishable from the Peters et al. patent.

Dependent claim 7 was objected to as being allowable. Appellants ask that the Board affirm the examiner's decision that dependent claim 7 is allowable if placed in independent form. Further, Appellants request the Board to find claim 1 allowable thereby making claim 7 allowable without amendment.

PAGE 11/21 * RCVD AT 6/28/2005 5:52:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:5129966854 * DURATION (mm-ss):05-58

Dependent claim 8 is dependent from claim 6 and recites that a line size of a replacement entry is selectively modified. Peters et al. do not disclose a prefetch buffer with a status field in the buffer lines. Peters et al. do not disclose the selective modification of buffer line length in response to a read request and clearly does not teach modification of line size of a replacement entry. The reference to Col. 4, lines 41-47 of Peters et al. in justifying the rejection of claim 8 is not relevant to the recited subject matter.

Dependent claims 9, 10 and 13 are each dependent at least from claim 8 and therefore the positions stated above are valid reasons for the allowable of these claims over the Peters et al. patent. Additionally, claims 9, 10 and 13 recite further features not taught by Peters et al. such as the modification of a status field in a prefetch buffer line.

Independent claim 14

Independent claim 14 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Peters et al. Since this rejection is based on the same reference, a repetition of the features of the Peters et al. system will not be made. Claim 14 recites "receiving a read request to a memory from a requesting master, the read request having a corresponding data size and burst length". The recited system of claim 14 noticeably differs from the Peters et al. system in which a master device issues a read command. Bridge control circuitry in the Peters et al. system then uses a stored value in a plurality of configuration registers to determine data transfer size associated with the master. Further, burst length information is not taught by the Peters et al. patent in connection with a read request. The Peters et al. patent also does not teach or suggest "providing a prefetch buffer configuration indicator based on the data size and the burst length". Further, the Peters et al. patent does not function as "based on the prefetch buffer reconfiguration indicator, selectively modifying total length of the replacement entry of the prefetch buffer based on an attribute of the read request to an adjusted line size". As mentioned above in connection

PAGE 12/21 * RCVD AT 6/28/2005 5:52:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:5129966854 * DURATION (mm-ss):05-58

with claim 1, the Peters et al. patent teaches the correlation of dedicated buffers having a fixed, non-varying line size to specific master devices and using configuration registers as a decoding mechanism to identify which fixed size buffer to use with which source or destination device. Claim 14 is improperly rejected under 35 U.S.C. 102(e) on the basis of Peters et al.

Dependent claims 15, 16 and 19

Dependent claims 15, 16 and 19 stand rejected under 35 U.S.C. § 102(e) as being unpatentable over Peters et al. Each of these claims is patentable over the combination of these references at least as a result of being dependent from claim 14 for the reasons provided above. Claim 15 was rejected on the basis of Col. 3, lines 37-42 as stated on page 6 of the Final Rejection. However, there is no teaching in this section of the Peters et al. patent of a "prefetch buffer reconfiguration indicator". The Peters et al. configuration registers hold size information that selects a predetermined prefetch buffer associated with the size as opposed to providing an indicator for "selectively modifying total length of the replacement entry of the prefetch buffer". There is no teaching in this section of the Peters et al. patent of a reconfiguration indicator based on "data size, the burst length, and a master identifier" as there is no buffer selection taught by Peters et al. based on burst length. A prima facie case of obviousness for claim 15 has not been made and is not supportable.

Dependent claim 16 recites "modifying at least one status field corresponding to the replacement entry". As detailed above, there is no teaching or suggestion within the Peters et al. patent of status fields in lines (entries) of a prefetch buffer. While the final rejection states the opposite, no citation reference from the Peters et al. patent which supports that statement is provided. Claim 16 recites "selectively modifying at least one status field corresponding to the replacement entry" of a prefetch buffer. The status and other PCI information stored by Peters et al. in the disclosed configuration registers does not perform or teach this function. Therefore, the recitals in claim 16 is not taught or suggested by the Peters et al. patent.

PAGE 13/21 * RCVD AT 6/28/2005 5:52:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:5129966854 * DURATION (mm-ss):05-58

Dependent claim 19 was rejected on the basis of step 506 of figure 5 of the Peters et al. patent. Step 506 therein states "receiving data transfer request from selected master device". As described by Peters et al., the prefetch buffer that receives a request is based on the stored size information that is correlated to a requesting master device. In contrast, claim 19 recites "wherein the at least one data fetch request is based on a bus width corresponding to the memory". Peters et al. does not teach this feature. The Peters et al. system has a source device, a destination device and a buffer. The size information stored in the Peters et al. system is described as size information of the source or destination device which is used to select a predetermined buffer. There is no teaching or suggestion within the Peters et al. patent to condition a data fetch request to a memory based upon "a bus width corresponding to the memory". Therefore, a prima facie case of obviousness for claim 19 has not been made and is not supportable.

Appellants' position described herein was dismissed in the final rejection because "the prior art need only show one buffer line at a time of different sizes, not different sizing of entire buffers". This position does not address the recital in claim 1 of "in response to the read request, selectively modifying total length of one or more prefetch buffer lines". This position does not address the recital in claim 14 of "providing a prefetch buffer reconfiguration indicator based on the data size and the burst length" (of the read request). Peters et al. do not teach these functions. Peters et al. size all buffers once in accordance with values in a configuration register and thereafter no size adjustment occurs in connection with any accesses. Rather, control circuitry routes data to or from one of those buffers whose size remains constant.

PAGE 14/21 * RCVD AT 6/28/2005 5:52:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:5129966854 * DURATION (mm-ss):05-58

Arguments for Ground 2

Dependent claims 17 and 18

Claims 17 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Peters et al. (cited supra) in view of Hicks et al. (U.S. Patent 6,085,291). In the rejection, Hicks et al. is cited for teaching an address tag field in figure 3 and figure 5. In the Hicks et al. system, data is prefetched in different ways depending upon a mode of operation. The address tag fields disclosed therein are conventional addresses used to address a line of cache memory. Dependent claim 17 is dependent from claim 16 and there is no teaching by Peters et al. and Hicks et al. for "selectively modifying at least one status field corresponding to the replacement entry" when "selectively modifying the total length of the replacement entry". Dependent claim 18 is dependent from claim 14 and there is no teaching by Peters et al. and Hicks et al. for "based on the prefetch buffer reconfiguration indicator, selectively modifying total length of the replacement entry of the prefetch buffer based on an attribute of the read request to an adjusted line size". While status fields and validity bits are known in the data processing field, the recited combination of features of claim 18 and claim 14 are not taught by the combination of Peters et al. and Hicks et al. The rejection of claims 17 and 18 is therefore improper.

For at least the reasons set forth above, Appellants respectfully submit that the claims of the present application are allowable over the art cited during prosecution.

Respectfully submitted,
Afzal Malik et al.

Robert L. King

Robert L. King
Attorney for Appellants
Reg. No. 30,185
Ph: (512) 996-6839

PAGE 15/21 * RCVD AT 6/28/2005 5:52:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:5129966854 * DURATION (mm-ss):05-58

Claims Appendix

1. (Previously Presented) A method for configuring a prefetch buffer, comprising:
receiving a read request from a master; and
in response to the read request, selectively modifying total length of one or more prefetch buffer lines of the prefetch buffer based on an attribute of the read request to an adjusted line size, thereby eliminating dedication of buffer storage to unused portions of the one or more prefetch buffer lines, the prefetch buffer having lines of differing total length during operation.

2. (Original) The method of claim 1, wherein the attribute of the read request comprises one of a master identifier corresponding to the master, a data size of the read request, and a burst length of the read request.

3. (Previously Presented) The method of claim 2, wherein selectively modifying the total length of one or more prefetch buffer lines is based on a second attribute of the read request, wherein the second attribute comprises another one of the master identifier, the data size, and the burst length.

4. (Original) The method of claim 1, wherein the read request results in a miss in the prefetch buffer.

5. (Original) The method of claim 1, wherein the prefetch buffer includes a plurality of lines, each of the plurality of lines having a corresponding one of status fields.

6. (Original) The method of claim 5, further comprising:
selecting at least a portion of the plurality of lines as a replacement entry within the prefetch buffer based on the status fields of the prefetch buffer.

7. (Original) The method of claim 6, wherein each of the status fields comprise an address tag field, an invalid field to indicate that a corresponding line in the prefetch buffer is not valid,

PAGE 16/21 * RCVD AT 6/28/2005 5:52:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:5129966854 * DURATION (mm-ss):05-58

a used field to indicate that a corresponding line in the prefetch buffer has been provided in response to a previous burst read request, and a valid field to indicate a corresponding line in the prefetch buffer has been provided in response to a previous non-burst read request.

8. (Previously Presented) The method of claim 6, wherein selectively modifying the total length of one or more prefetch buffer lines comprises selectively modifying a line size of the replacement entry.

9. (Original) The method of claim 8, wherein selectively modifying the line size of the replacement entry comprises selectively modifying a status field corresponding to the replacement entry.

10. (Original) The method of claim 9, wherein selectively modifying the status field corresponding to the replacement entry is based on the attribute of the read request, the attribute comprising at least one of a data size and a burst length of the read request.

Claims 11 and 12 (Canceled)

13. (Original) The method of claim 10, further comprising:

generating at least one data request to a memory addressed by the read request; and

storing data from the memory into the replacement entry of the prefetch buffer.

14. (Previously Presented) A method for configuring a prefetch buffer, comprising:

receiving a read request to a memory from a requesting master, the read request having a corresponding data size and burst length;

providing a prefetch buffer reconfiguration indicator based on the data size and the burst length;

selecting a replacement entry within the prefetch buffer;

based on the prefetch buffer reconfiguration indicator, selectively modifying total length of the replacement entry of the prefetch buffer based on an attribute

PAGE 17/21 * RCVD AT 6/28/2005 5:52:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:5129966854 * DURATION (mm-ss):05-58

of the read request to an adjusted line size that eliminates dedicating unused buffer storage to the replacement entry of the prefetch buffer; and

storing data fetched from the memory in the replacement entry.

15. (Original) The method of claim 14, wherein the prefetch buffer reconfiguration indicator is based on the data size, the burst length, and a master identifier corresponding to the requesting master.

16. (Previously Presented) The method of claim 14, wherein selectively modifying the total length of the replacement entry comprises selectively modifying at least one status field corresponding to the replacement entry.

17. (Original) The method of claim 16, wherein the at least one status field comprises an address tag field, wherein selectively modifying the at least one status field comprises selectively modifying the address tag field.

18. (Original) The method of claim 14, wherein selecting the replacement entry within the prefetch buffer comprises checking at least one of valid, invalid, or used bits within status fields of the prefetch buffer.

19. (Original) The method of claim 14, further comprising:

generating at least one data fetch request to the memory, wherein the at least one data fetch request is based on a bus width corresponding to the memory.

20. (Allowed) A data processing system, comprising:

a master;

a memory;

a prefetch buffer, coupled to the master and the memory, the prefetch buffer having a plurality of lines and status fields, each of the plurality of lines having a corresponding one of the status fields, each of the status fields comprises an address tag field, an invalid field to indicate that a

PAGE 18/21 * RCVD AT 6/28/2005 5:52:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:5129966854 * DURATION (mm-ss):05-58

corresponding line in the prefetch buffer is not valid, a used field to indicate that a corresponding line in the prefetch buffer has been provided in response to a previous burst read request, and a valid field to indicate a corresponding line in the prefetch buffer has been provided in response to a previous non-burst read request; and

prefetch control circuitry coupled to the prefetch buffer, the prefetch control circuitry, in response to a read request from the master, selectively modifying a line size of at least a portion of the prefetch buffer.

21. (Allowed) The data processing system of claim 20, wherein the prefetch control circuitry selects a replacement entry within the prefetch buffer, and selectively modifying the line size comprises selectively modifying a line size of the replacement entry.

22. (Allowed) The data processing system of claim 21, wherein the prefetch control circuitry receives a data size indicator and a burst length indicator from the master and selectively modifies the line size of the replacement entry based on the data size indicator and the burst length indicator.

Claims 23 and 24 (Canceled)

PAGE 19/21 * RCVD AT 6/28/2005 5:52:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:5129966854 * DURATION (mm-ss):05-58

Evidence Appendix Under 37 CFR 41.37(c)(1)(ix)

There is no evidence that has been entered into the record by the Examiner that is relied upon in this appeal.

PAGE 20/21 * RCVD AT 6/28/2005 5:52:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:5129966854 * DURATION (mm-ss):05-58

RELATED PROCEEDINGS APPENDIX

There are no related proceedings.

PAGE 21/21 * RCVD AT 6/28/2005 5:52:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:5129966854 * DURATION (mm-ss):05-58